REMARKS

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claims 1-8 and 12-15 are pending in this application. Claim 1 and claim 14 are amended herein. Claim 11 is canceled herein. No claims have been allowed.

Within the Detailed Action, paragraph 1, of the office action mailed 30 August 2002, applicant respectfully disagrees with the Examiner's assessment that applicant has canceled claims 1 and 14-15 within this application. Rather, within applicant's communication dated 20 May 2002 applicant has amended claim 1 and 11, canceled claims 9-10 and newly added claims 14-15. Thus, applicant asserts, that claims 1-8 and 11-15 were pending in this application prior to applicant's amendment of claims 1 and 14, and deletion of claim 11, as above.

Within the Detailed Action, paragraph 2, of the office action mailed 30 August 2002, applicant believes that no final rejection was previously imposed within this application and thus no final rejection may presumably be withdrawn within this application.

Claim Rejections - 35 U.S.C. § 103

1. The Examiner has rejected claims 3-7 and 11-13 under 35 U.S.C. § 103(a) as being unpatentable over Kelly et al. (U.S. Patent No. 6,143,117; hereinafter "Kelly") in view of Haq (U.S. Patent No. 6,245,677) and Mountain (U.S. Patent No. 6,013,534).

In accord with applicant's understanding of claims pending within this application, applicant assumes that the Examiner might have intended rejection of claims 1, 3-7 and 11-13 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Haq and Mountain, since the Examiner has not otherwise rejected an independent base claim from which other claims depend.

Applicant also notes that Haq has apparently not properly been made of record and cited on form PTO-892, nor has a copy of Haq been supplied with the office action mailed on 30 August 2002. Applicant has obtained independently a copy of Haq and will nonetheless respond to the foregoing claim rejections.

In response, applicant has twice amended claim 1 to incorporate therein the limitations from amended claim 11, while canceling amended claim 11, to provide within twice amended claim 1 limitations which applicant believes to patentably distinguish applicant's invention from that which is disclosed within Kelly, Haq, Mountain or the combination thereof. MPEP 2143, 2143.03.

In that regard, applicant has twice amended claim 1 to incorporate therein the limitation that applicant's second substrate is removed from applicant's laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, and while employing applicant's dielectric isolated metallization pattern as a stop layer.

In comparison, applicant first notes that the Examiner at page 3, last paragraph, of the office action mailed on 30 August 2002 acknowledges that Kelly does not disclose removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods.

In addition, applicant next notes that while Haq, as cited by the Examiner, does disclose a polishing method for backside thinning a substrate, such as a semiconductor substrate, Haq does not apparently require a dielectric isolated metallization pattern be formed upon Haq's substrate prior to thinning thereof, nor does Haq disclose employing the dielectric isolated metallization pattern as a stop layer when thinning Haq's substrate. Applicant further notes that Haq's invention is preferably employed with the context of a semiconductor substrate having defined on the front side thereof live circuits which presumably may include a dielectric isolated metallization pattern such as to access semiconductor devices employed within the live circuits and formed within the semiconductor substrate (col. 3, lines 18-24). Under such circumstances where a semiconductor substrate having formed therein semiconductor devices and formed thereupon a dielectric isolated metallization pattern to access the semiconductor devices and live circuits formed therefrom is completely thinned and removed while employing the dielectric isolated metallization pattern as a stop layer, Haq's invention is rendered inoperative for its intended purpose since such complete thinning and removal of Haq's semiconductor substrate would also remove Haq's semiconductor devices and render inoperative Haq's live circuits. Thus, in addition to not providing each and every limitation within applicant's invention as disclosed and claimed within twice amended claim 1, Haq if extended to provide limitations in accord with applicant's invention may not properly be combined with Kelly to reject any of

applicant's claims to applicant's invention, since Haq is rendered inoperative upon such extension. MPEP 2143, 2143.01. Applicant finally notes that Haq apparently teaches away from applicant's claim 12 and for that reason also may not properly be employed in rejecting any of applicant's claims to applicant's invention. MPEP 2141, 2141.02.

Finally, while Mountain, as cited by the Examiner, does disclose an etch stop layer for use when removing a substrate from a thinned semiconductor integrated circuit microelectronic fabrication die, Mountain's etch stop layer does not comprise a dielectric isolated metallization pattern employed within a semiconductor integrated circuit microelectronic fabrication, but rather is an extrinsically formed etch stop layer formed specifically for etch stop purposes (col. 4, line 63 to col. 5, line 13).

Thus, since each and every limitation within applicant's invention as disclosed and claimed within twice amended claim 1 is not disclosed within Kelly, Haq or Mountain or the combination thereof, and since Haq's invention would be rendered inoperative for Haq's intended purpose if extended to provide a limitation in accord with applicant's invention, applicant asserts that twice amended claim 1 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Haq and Mountain.

Since all remaining claims within the foregoing rejections are dependent upon twice amended claim 1 and carry all of the limitations of twice amended claim 1, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Haq and Mountain.

2. The Examiner has rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Haq and Mountain, and further in view of Davidson (U.S. Patent No. 5,880,010).

3. The Examiner has rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Haq and Mountain, and further in view of Kresge et al. (U.S. Patent No. 6,066,808; hereinafter "Kresge").

While not precluding the existence of independent patentable distinctions between:: (1) Kelly in view of Haq and Mountain: and (a) Davidson; or (b) Kresge; and (2) that which is claimed within claim 2 and claim 8, applicant predicates patentability of claim 2 and claim 8 upon their dependence upon twice amended claim 1.

In light of the foregoing responses, applicant respectfully requests that the Examiner's rejections of: (1) claims 3-7 and 11-13 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Haq and Mountain; (2) claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Haq and Mountain, and further in view of Davidson; and (3) claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Haq and Mountain, and further in view of Kresge, be withdrawn.

Other Considerations

Applicant has amended claim 14 to correspond with twice amended claim 1, but with the additional limitation that applicant's partially fabricated semiconductor integrated circuit microelectronic fabrication and applicant's second substrate are pressure laminated. Although

the Examiner has not apparently provided any basis for rejection of applicant's claims 14-15, applicant asserts patentability of applicant's amended claim 14 predicated upon the same reasons as applicant asserts patentability of applicant's twice amended claim 1. Applicant asserts patentability of applicant's claim 15 upon its dependence upon applicant's amended claim 14.

The Examiner has cited no additional prior art of record not employed in rejecting applicant's claims to applicant's invention.

No fee is due as a result of this amendment and response.

SUMMARY

Applicant's invention as disclosed and claimed within twice amended claim 1 and amended claim 14 provides a laminating method for forming a microelectronic fabrication. The laminating method laminates a partially fabricated semiconductor integrated circuit microelectronic fabrication with a dielectric isolated metallization pattern formed in inverted order over a second substrate. The second substrate is then removed employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, and while employing the dielectric isolated metallization pattern as a stop layer. Absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention as disclosed and claimed within twice amended claim 1 and amended claim 14.

CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

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APPENDIX

COMPLETE COPY OF THE CLAIMS

(MARKED-UP WITH CURRENT REVISIONS)

1. (twice amended) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication;

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication; and

removing the second substrate from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, and while employing the dielectric isolated metallization pattern as a stop layer.

2. The method of claim 1 wherein the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors.

3. The method of claim 1 wherein the second substrate is selected from the group consisting of conductor substrates, semiconductor substrates, dielectric substrates and aggregates thereof.

4. The method of claim 1 wherein the second substrate is a second semiconductor substrate.

5. The method of claim 1 wherein the first semiconductor substrate is thicker than the second substrate.

6. The method of claim 1 wherein the dielectric isolated metallization pattern comprises a plurality of laminated patterned conductor layers.

7. The method of claim 6 wherein each laminated patterned conductor layer within the plurality of laminated patterned conductor layers is formed to a thickness of from about 3000 to about 6000 angstroms.

8. The method of claim 1 wherein the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern formed over the second substrate is undertaken while employing a laminating method selected from the group consisting of thermally assisted laminating methods and pressure assisted laminating methods.

9. - 11. (canceled)

12. The method of claim 1 wherein the semiconductor substrate is not thinned after forming thereover the minimum of one microelectronic device.

13. The method of claim 1 wherein the second substrate is not removed from the dielectric isolated metallization pattern prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern.

14. (amended) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication; [and]

pressure laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a pressure laminated completely fabricated semiconductor integrated circuit microelectronic fabrication; and

removing the second substrate from the pressure laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, and while employing the dielectric isolated metallization pattern as a stop layer.

15. The method of claim 14 wherein the partially fabricated semiconductor integrated circuit microelectronic fabrication and the second substrate are pressure laminated while employing a bonding material selected from the group consisting of indium and indium alloy bonding materials.